IN THE CLAIMS

Re-write Claims 1, 3-9, 11-12 and 20 as follows.
Cancel Claim 2.

1.   (currently amended) A semiconductor memory device
comprising:

a memory array configured to store data values and
corresponding error correction code values; ~~and~~

a first register configured to store a first write
data value and a corresponding first write address
value during a first write access to the memory array;

~~a write buffer/~~ an error correction code (ECC)
generator configured to receive ~~and store a~~ the first
write data value from the first register, and in
response, ~~and a corresponding write address value, and~~
generate ~~an~~ a first ECC value ~~in response to the write
data value~~ during ~~the~~ a first write access to the
memory array, the ECC generator being configured to
provide the first ECC value as long as the first write
data value is stored in the first register; ~~and~~

means for outputting the first write data value
and the first ECC value during a read access if a read
address value associated with the read access matches
the first write address value stored in the first
storage circuit; and

means for writing ~~routing~~ the first write data
value~~, write address value~~ and the first ECC value to a
location in the memory array associated with the first
write address value during a second write access.

2.   (canceled)

3. (currently amended) The semiconductor memory device of Claim 1 ~~2~~, ~~wherein the write buffer/ECC generator~~ further ~~comprises~~ comprising a second register configured to receive and store the first write data value and the corresponding first write address value from the first register, and the first ECC value from the error correction code generator, the second register being coupled to the memory array.

4. (currently amended) The semiconductor memory device of Claim 1 ~~2~~, wherein the ~~write buffer/ECC generator further~~ means for outputting comprises a comparator coupled to receive the first write address value stored in the first register and the read address value associated with the read access ~~a write~~ ~~address value applied to the first register~~, the comparator asserting a match control signal when the first write address value matches the read address value associated with the read access ~~values match~~.

5. (currently amended) The semiconductor memory device of Claim 4, wherein the ~~write buffer/ECC generator~~ means for outputting further comprises a logic circuit coupled to receive the match control signal and a read enable signal, the logic circuit ~~gate~~ asserting a hit signal to indicate that a read access has hit the ~~write buffer/ECC~~ ~~generator~~ first register when the match control signal and the read enable signal are both asserted.

6. (currently amended) The semiconductor memory device of Claim 2 ~~1~~, wherein the ~~write buffer/ECC generator~~ first register and the second register form ~~comprises~~ a

double buffered write-buffer arranged in a first in, first out (FIFO) configuration.

      7.   (currently amended) The semiconductor memory device of Claim 1, wherein ~~the write buffer/ECC generator comprises:~~ <u>the first register is further configured to store a second write data value and a corresponding second address value during the second write access to the memory array, and wherein the error correction code (ECC) generator is further configured to receive the second write data value from the first register, and in response, generate a second ECC value during the second write access to the memory array</u> ~~means for storing a write data value and a write address value of a present write transaction; and~~

~~means for retiring a write data value and ECC value associated with a previous write transaction to a location in the memory array designated by a write address value associated with the previous write transaction.~~

      8.   (currently amended) A method of operating a semiconductor memory comprising:

      storing a first write data value and a corresponding first write address in a first stage of a write buffer during a first write access;

      generating a first error correction code (ECC) value in response to the first write data value stored in the first stage of the write buffer during the first write access <u>and providing the first ECC value as long as the first write data value is stored in the first register</u>; ~~and~~

transferring the first write data value, the first
ECC value and the first write address to a memory array
during a second write access;

~~retiring~~ writing the first write data value and
the first ECC value to a location in the memory array
identified by the first write address during the second
write access;

storing a second write data value and a
corresponding second write address in the first stage
of ~~a~~ the write buffer during the second write access;
and

generating a second error correction code (ECC)
value in response to the second write data value stored
in the first stage of the write buffer during the
second write access and providing the second ECC value
as long as the second write data value is stored in the
first register.

9.   (currently amended) The method of Claim 8,
further comprising:

transferring the first write data value, the first
ECC value and the first write address into a second
stage of the write buffer during the second write
access; and

~~retiring~~ writing the first write data value and
the first ECC value from the second stage of the write
buffer to the location in the memory array identified
by the first write address during the second write
access.

10.   (original) The method of Claim 8, further
comprising driving the first write data value and the first

ECC value to the memory array by enabling tri-state buffers
during the second write access.

11.   (currently amended)   The method of Claim 8,
further comprising ~~asserting a write buffer hit signal~~
<u>outputting the first write data value and the first ECC</u>
<u>value</u> if a read address of a read access matches ~~a~~ <u>the first</u>
write address <u>value</u> stored in the first stage of the write
buffer.

12.   (currently amended)   The method of Claim 11,
further comprising inhibiting access to the memory array <u>if</u>
<u>a read address of a read access matches the first write</u>
<u>address value stored in the first stage of the write buffer</u>
~~when the write buffer hit signal is asserted~~.

13.   (original)   A semiconductor memory device
comprising:

        a memory array configured to store data/error
    correction code (ECC) values, wherein each data/ECC
    value includes a data value and a corresponding error
    correction code (ECC) value;

        an error detection/correction circuit coupled to
    receive a first data/ECC value from a first address of
    the memory array during a first read access, the error
    detection/correction circuit being configured to
    generate a corrected first data/ECC value and assert an
    error indicator signal upon detecting an error in the
    first data/ECC value; and

        a write-back buffer configured to store the
    corrected first data/ECC value in response to the
    asserted error indicator signal, the write-back buffer

further being configured to write the corrected first data/ECC value to the first address of the memory array during an idle cycle of the memory device.

14. (original) The semiconductor memory device of Claim 13, wherein the write-back buffer includes multiple entries, and is arranged in a first in, first out (FIFO) configuration.

15. (original) The semiconductor memory device of Claim 13, wherein the write-back buffer includes multiple entries, and is arranged in a last in, first out (LIFO) configuration.

16. (original) The semiconductor memory device of Claim 13, wherein the write-back buffer includes multiple entries, the write-back buffer including a circuit to prevent write operations to the write-back buffer when all of the entries of the write-back buffer are full.

17. (original) A method of operating a semiconductor device, the method comprising:

storing a plurality of data/error correction code (ECC) values in a memory array, wherein each data/ECC value includes a data value and a corresponding error correction code (ECC) value;

generating a first corrected data/ECC value in response to a first data/ECC value retrieved from a first address of the memory array during a first read access, wherein the first data/ECC value includes an error;

asserting an error indicator signal to indicate that the first data/ECC value includes an error;

storing the first corrected data/ECC value and the first address in a write-back buffer in response to the asserted error indicator signal; and

writing the first corrected data/ECC value to the first address of the memory array during an idle cycle of the memory device.

18. (original) The method of Claim 17, further comprising:

generating a second corrected data/ECC value in response to a second data/ECC value retrieved from a second address of the memory array during a second read access, wherein the second data/ECC value includes an error;

asserting the error indicator signal to indicate that the second data/ECC value includes an error;

storing the second corrected data/ECC value and the second address in the write-back buffer in response to the asserted error indicator signal, wherein the first corrected data/ECC value and the second corrected data/ECC value are stored in the write-back buffer at the same time; and

writing the second corrected data/ECC value to the second address of the memory array during an idle cycle of the memory device.

19. (original) A semiconductor memory device comprising:

a memory array configured to store data/error correction code (ECC) values, wherein each data/ECC

value includes a data value and a corresponding error
correction code (ECC) value;

a write buffer/error correction code (ECC)
generator configured to receive and store a write data
value and a corresponding write address value, and
generate an ECC value in response to the write data
value during a first write access;

circuitry for routing the write data value, write
address value and ECC value to the memory array during
a second write access;

an error detection/correction circuit coupled to
receive a first data/ECC value from a first address of
the memory array during a first read access, the error
detection/correction circuit being configured to
generate a corrected first data/ECC value and assert an
error indicator signal upon detecting an error in the
first data/ECC value; and

a write-back buffer configured to store the
corrected first data/ECC value in response to the
asserted error indicator signal, the write-back buffer
further being configured to write the corrected first
data/ECC value to the first address of the memory array
during an idle cycle of the memory device.

20.   (currently amended) A method of operating a
semiconductor memory comprising:

storing a first write data value and a
corresponding first write address in a first stage of a
write buffer during a first write access;

generating a first error correction code (ECC)
value in response to the first write data value stored

in the first stage of the write buffer during the first write access;

transferring the first write data value, the first ECC value and the first write address into a second stage of the write buffer during a second write access;

~~retiring~~ writing the first write data value and the first ECC value from the second stage of the write buffer to a first address ~~location~~ in a memory array identified by the first write address during the second write access;

~~storing a second write data value and a corresponding second write address in the first stage of a write buffer during the second write access;~~

~~generating a second ECC value in response to the second write data value stored in the first stage of the write buffer during the second write access;~~

~~storing a plurality of data/ECC values in the memory array, wherein each data/ECC value includes a data value and a corresponding ECC value;~~

reading the first write data value and the first ECC value from the first address of the memory array;

generating a first corrected data/ECC value in response to the first write data value and the first ECC value ~~a first data/ECC value~~ retrieved from ~~a first address of~~ the memory array ~~during a first read access~~, wherein the first write data value and the first ECC value ~~data/ECC value~~ includes an error;

asserting an error indicator signal to indicate that the first write data value and the first ECC value ~~data/ECC value~~ includes an error;

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storing the first corrected data/ECC value and the first address in a write-back buffer in response to the asserted error indicator signal; and

writing the first corrected data/ECC value to the first address of the memory array during an idle cycle of the memory device.